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DIGITAL SIGNAL PROCESSOR BASED ON JUMPING FLOATING-POINT ARITHMETIC

Abstract

A digital signal processor for processing a plurality of digital data in a fixed-point representation or a jumping floating-point representation. The digital signal processor includes a multiplication circuit, an extracting/shifting device, a plurality of representation converters, and an arithmetic unit. The multiplication circuit is used to generate a long bit-length digital data by multiplying two short bit-length digital data with each other. The extracting/shifting device is electrically connected to the multiplication circuit for transforming the long bit-length digital data in jumping floating-point representation to a long bit-length digital data in fixed-point representation. Each representation converter is used to transform a digital data between the fixed-point representation and the jumping floating-point representation. The arithmetic unit is used to operate a plurality of digital data.